

FIGURE 1 (Prior Art)

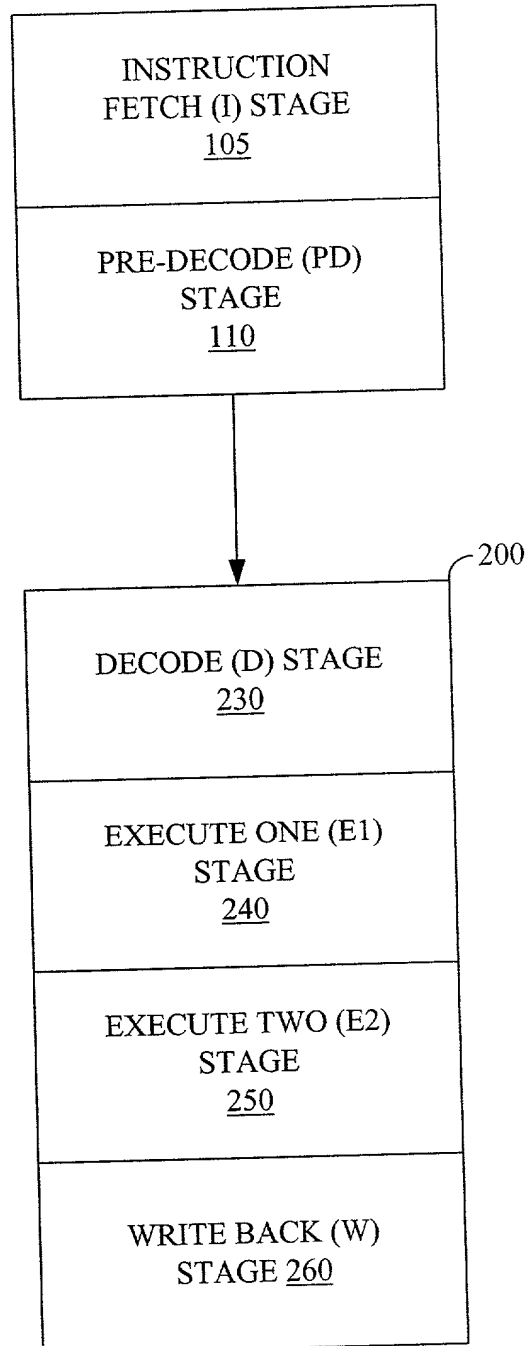


FIGURE 2 (Prior Art)

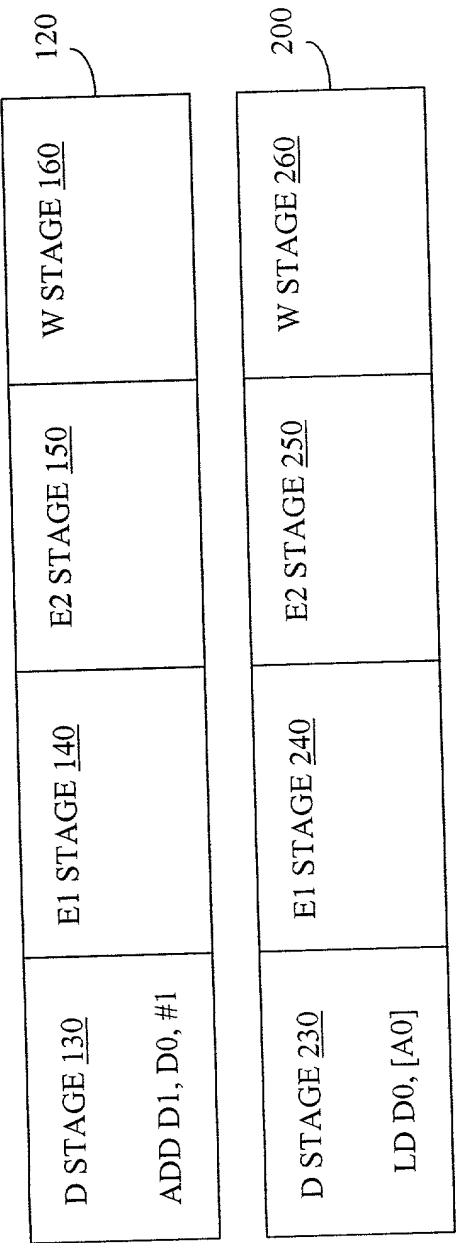


Figure 3(a)

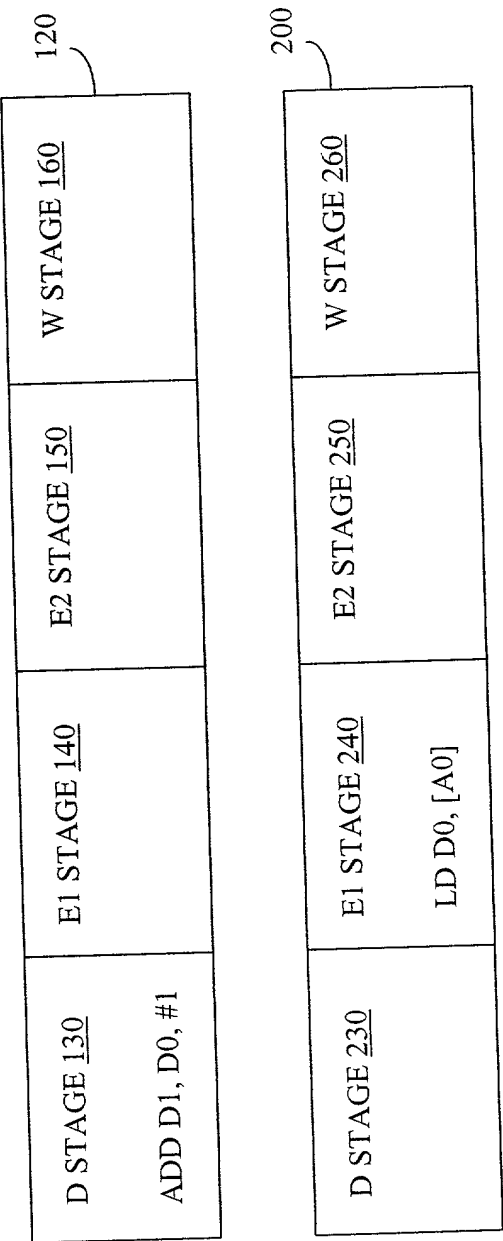


Figure 3(b)

FIG. 3(c) is a block diagram of a processor 120, according to one embodiment. The processor 120 includes a D stage 130, an E1 stage 140, an E2 stage 150, and a W stage 160. The D stage 130 is configured to add D1, D0, #1. The E1 stage 140 is configured to add D1, D0, #1. The E2 stage 150 is configured to add D1, D0, #1. The W stage 160 is configured to add D1, D0, #1.

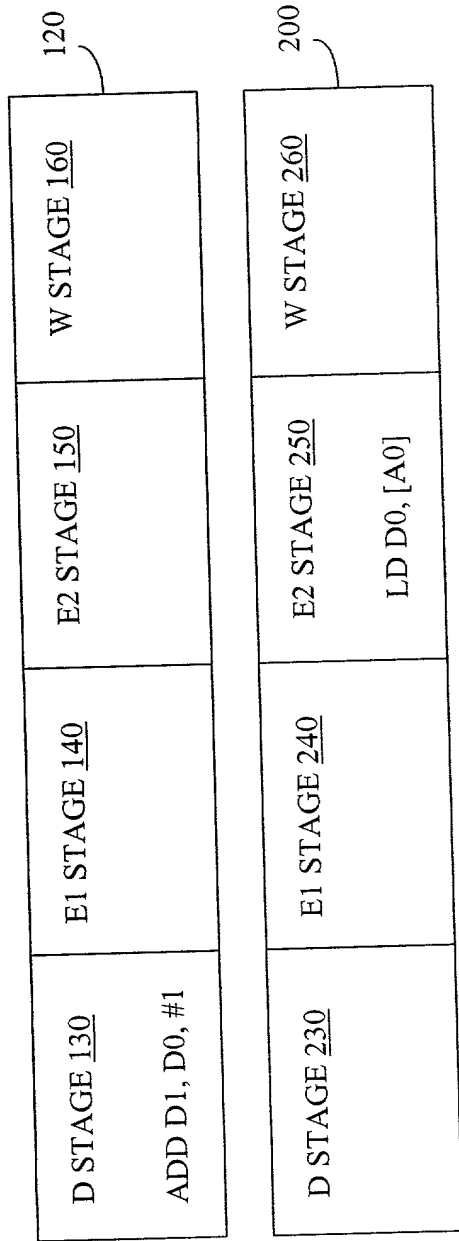


Figure 3(c)

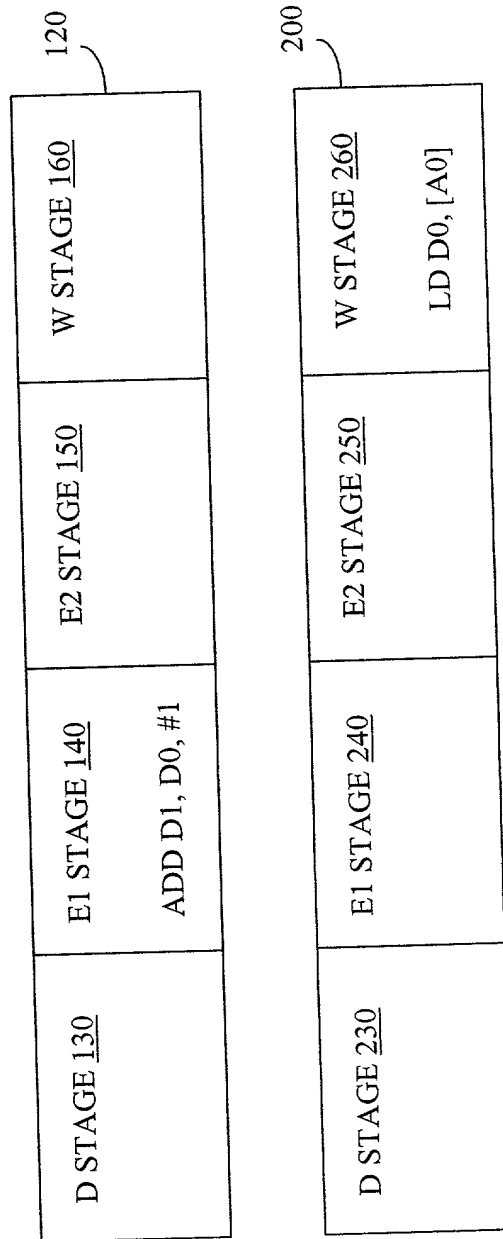


Figure 3(d)

FIG. 3(e) is a block diagram of a processor 100 showing a pipeline with four stages: D STAGE 130, E1 STAGE 140, E2 STAGE 150, and W STAGE 160. The E2 STAGE 150 is labeled with the instruction "ADD D1, D0, #1". The processor 100 is also labeled with the number 120.

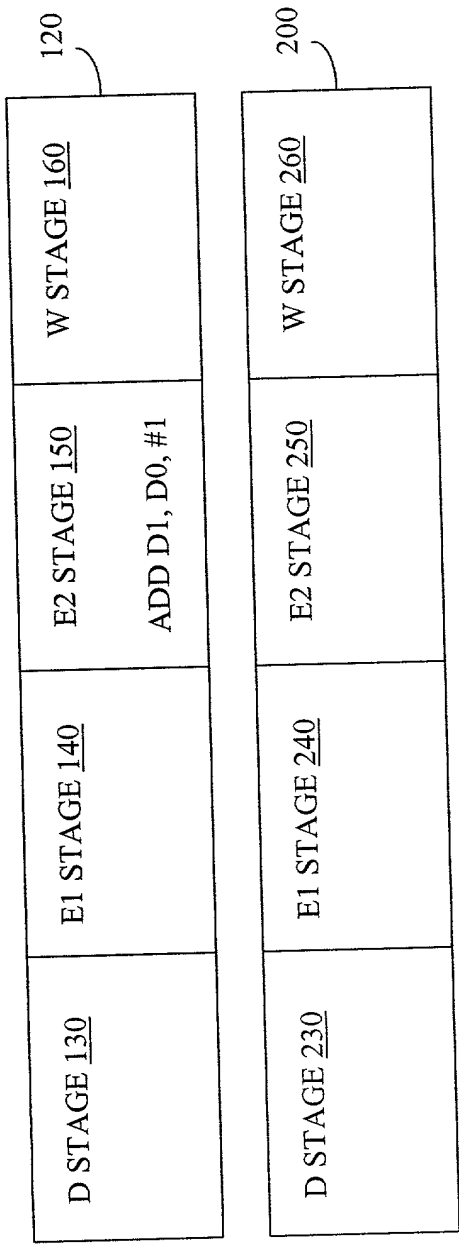


Figure 3(e)

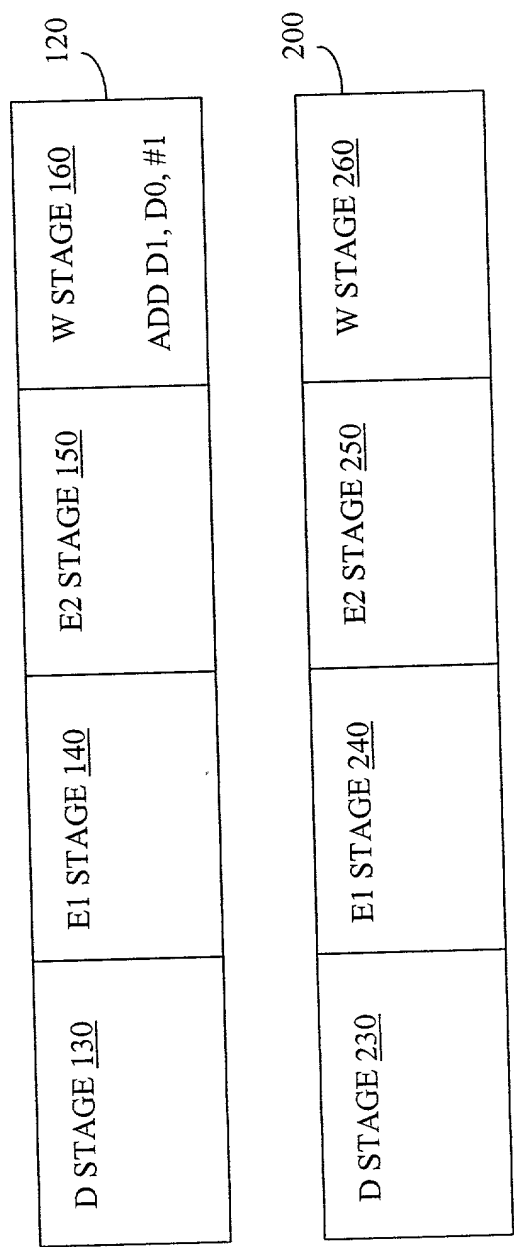


Figure 3(f)

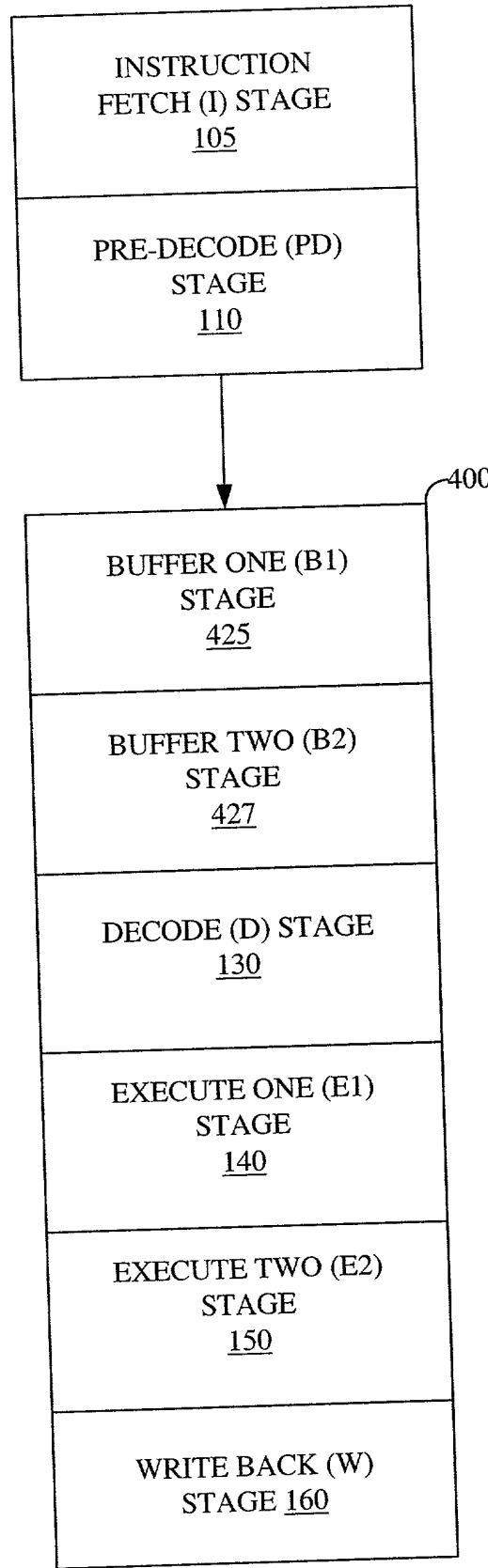


FIGURE 4 (Prior Art)

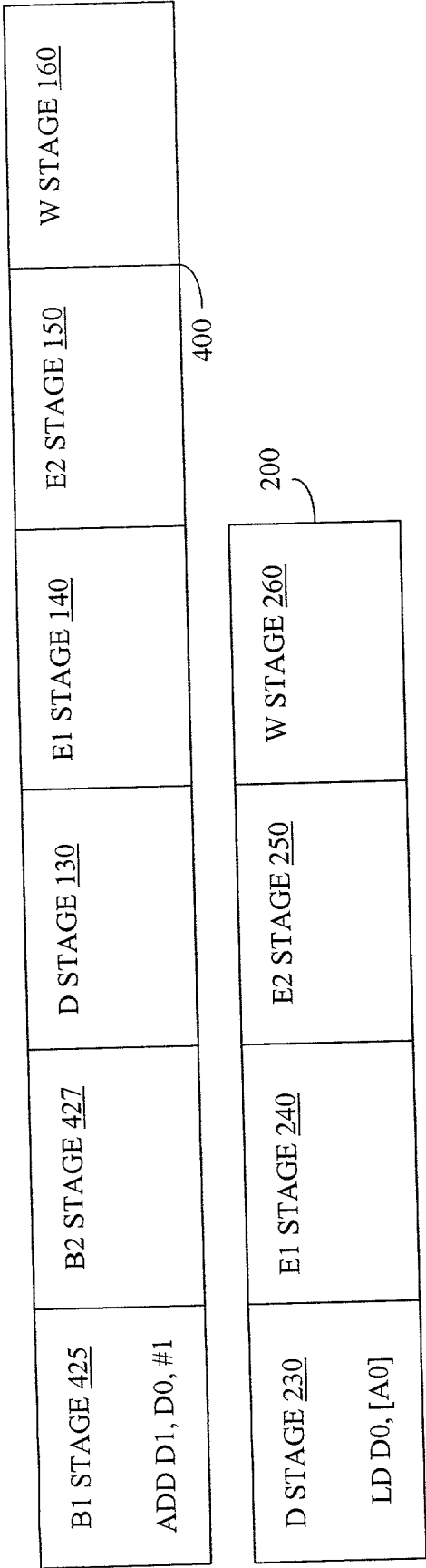


Figure 5(a)

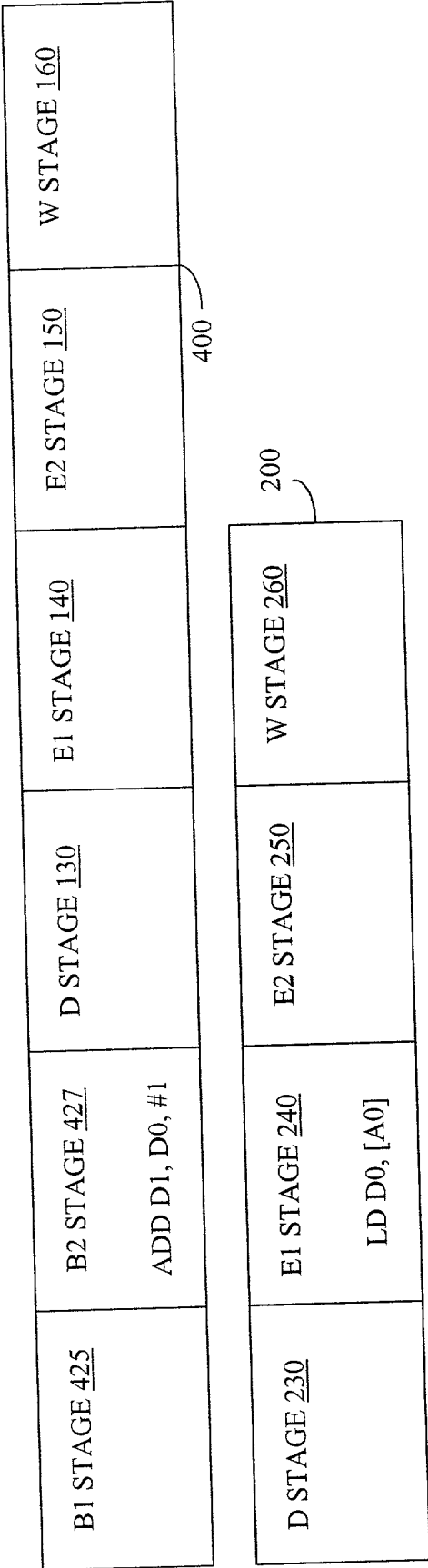


Figure 5(b)

FIG. 5(c) is a block diagram of a processor 400, according to one embodiment of the present invention. The processor 400 includes a B1 stage 425, a B2 stage 427, a D stage 430, an E1 stage 140, an E2 stage 150, and a W stage 160. The B1 stage 425 is connected to the B2 stage 427, which is connected to the D stage 430. The D stage 430 is connected to the E1 stage 140, which is connected to the E2 stage 150, which is connected to the W stage 160. The E1 stage 140 is labeled "ADD D1, D0, #1". The E2 stage 150 is labeled "LD D0, [A0]". The W stage 160 is labeled "LD D0, [A0]".

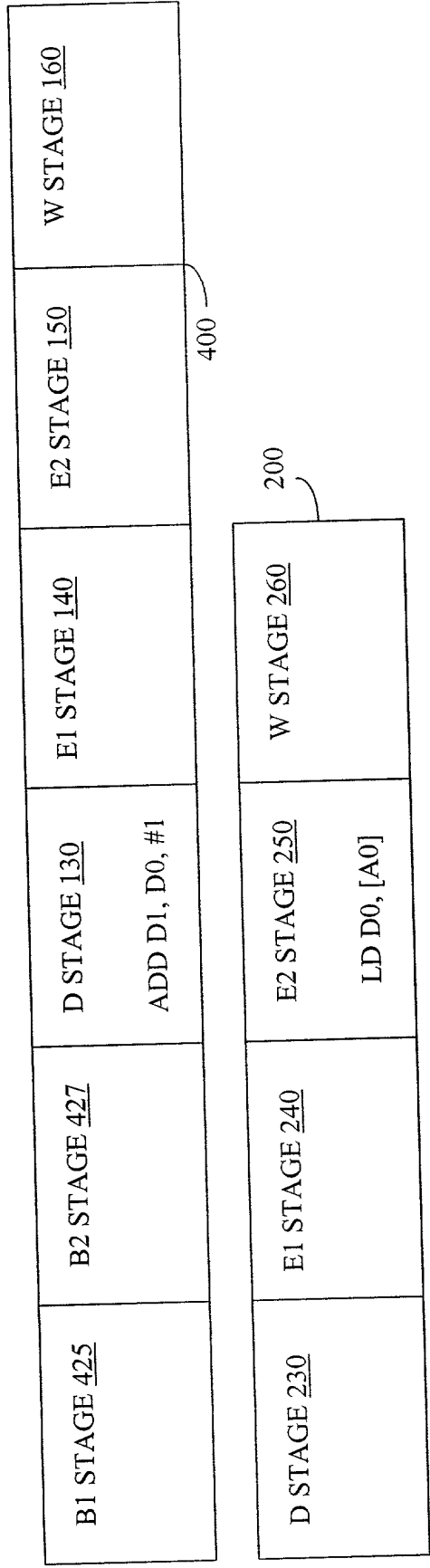


Figure 5(c)

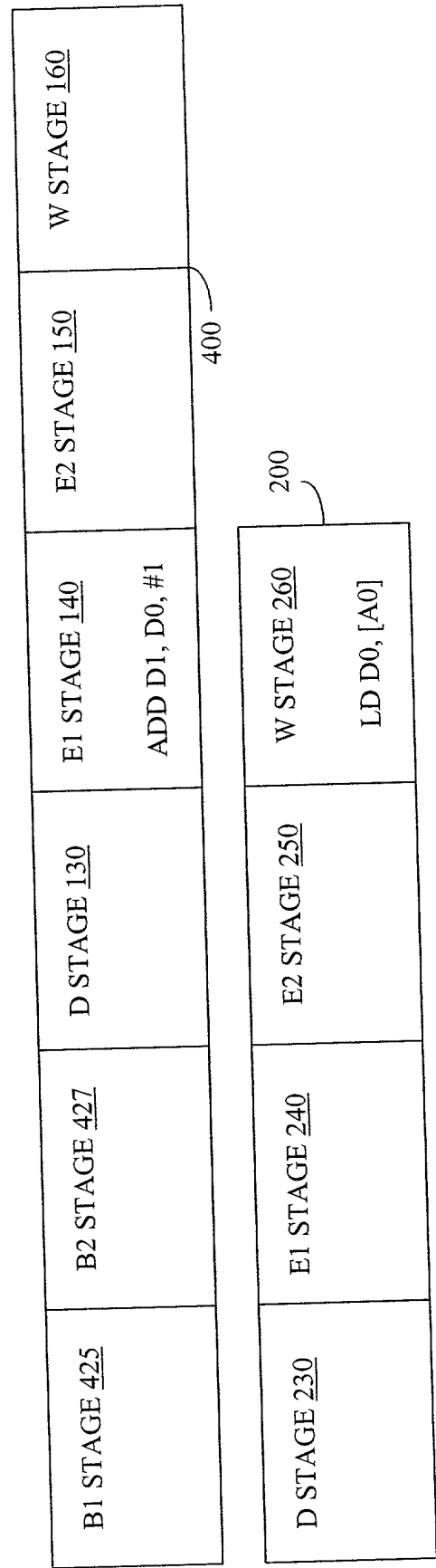


Figure 5(d)

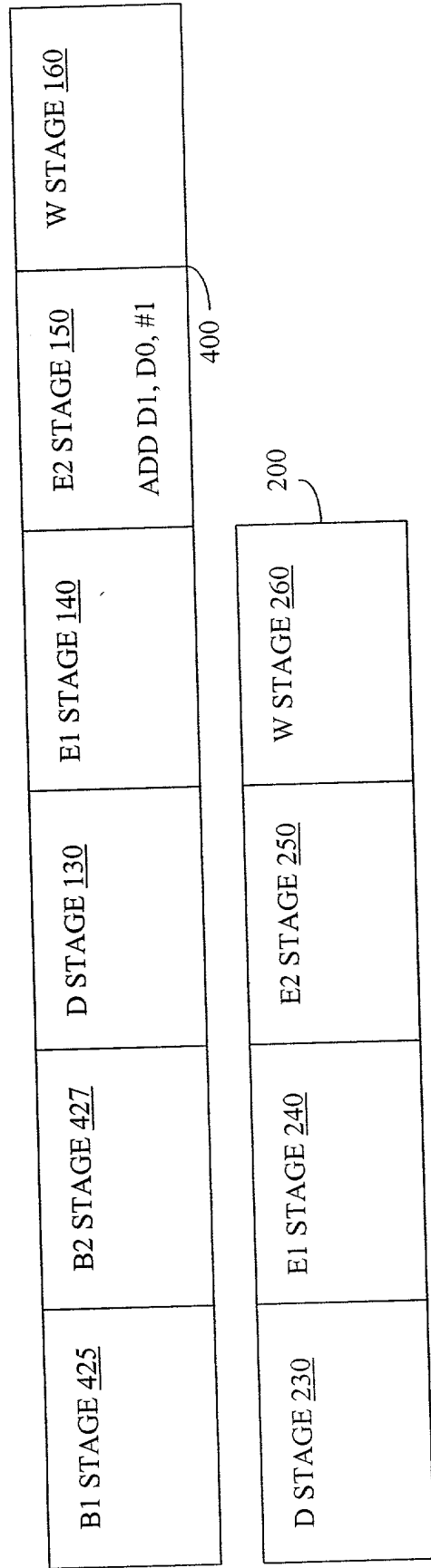


Figure 5(e)

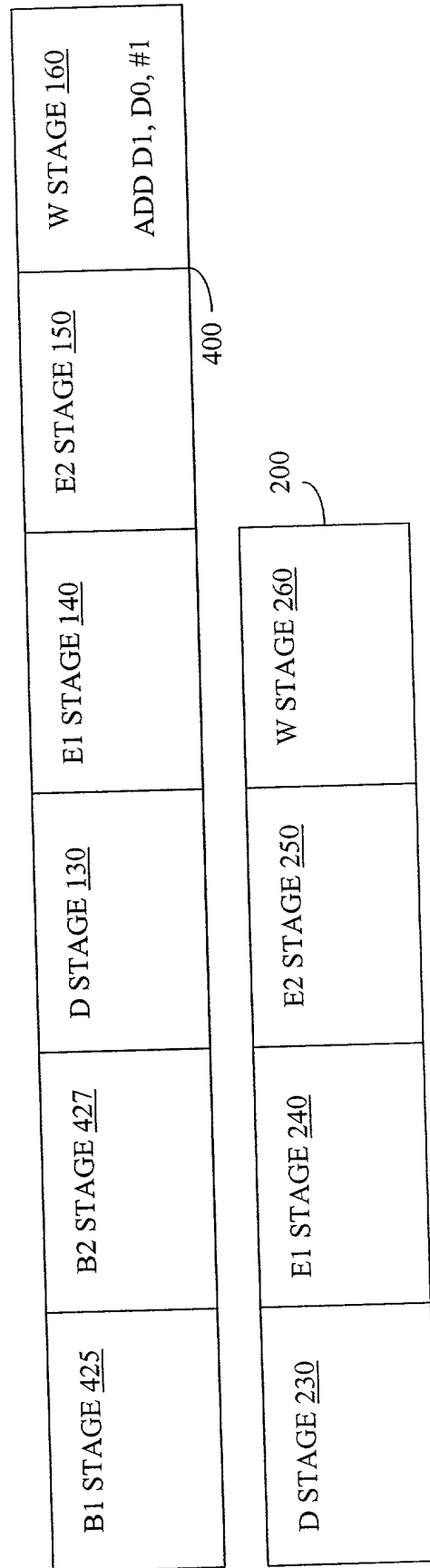


Figure 5(f)

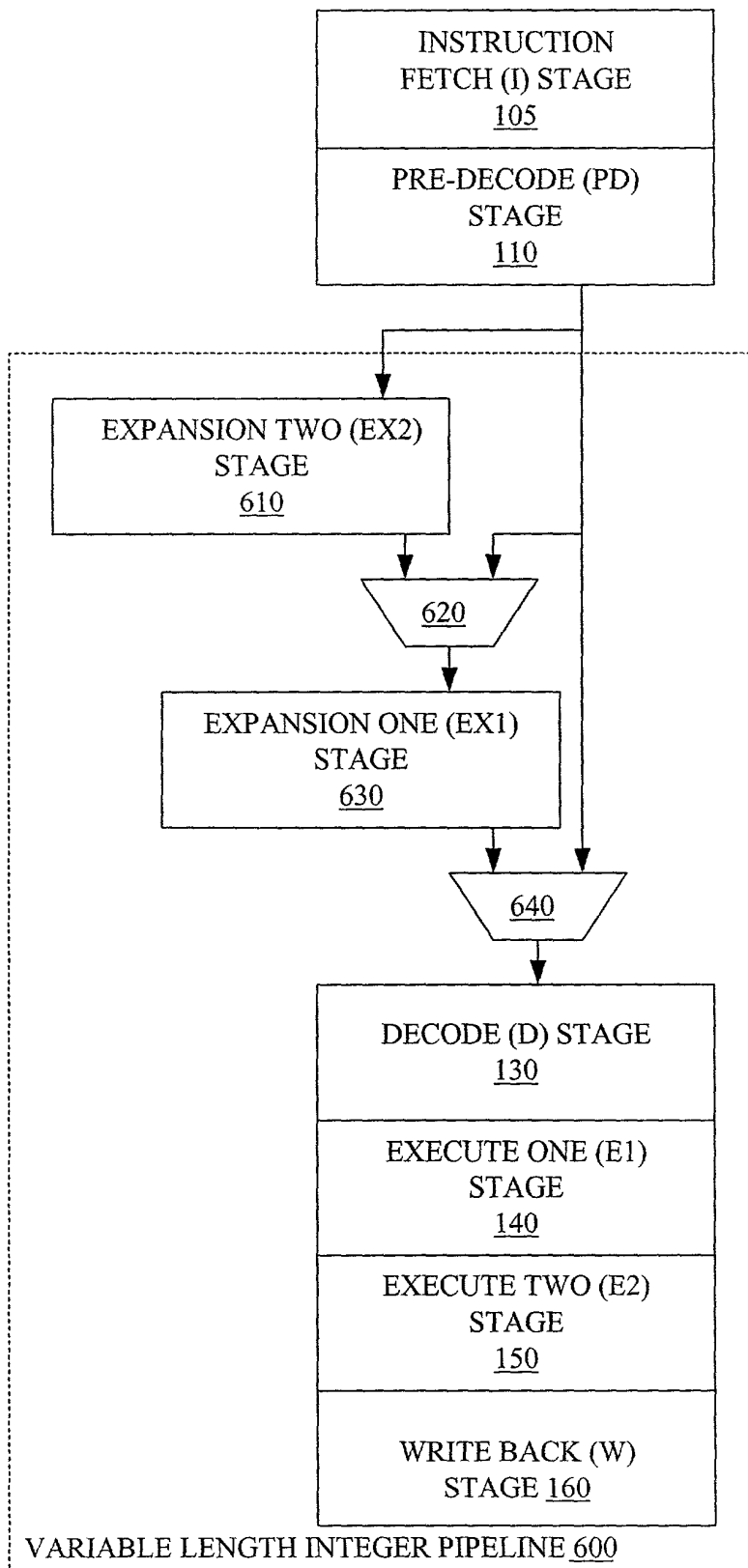


FIGURE 6

FIG. 7(a) is a block diagram of a processor 200 showing a pipeline with four stages: D STAGE 130, E1 STAGE 140, E2 STAGE 150, and W STAGE 160. The D STAGE 130 performs SUB D3, D1, #1. The E1 STAGE 140 performs E1 STAGE 140. The E2 STAGE 150 performs E2 STAGE 150. The W STAGE 160 performs W STAGE 160. A bracket labeled 600 spans the E1 and E2 stages. A bracket labeled 200 spans the entire pipeline.

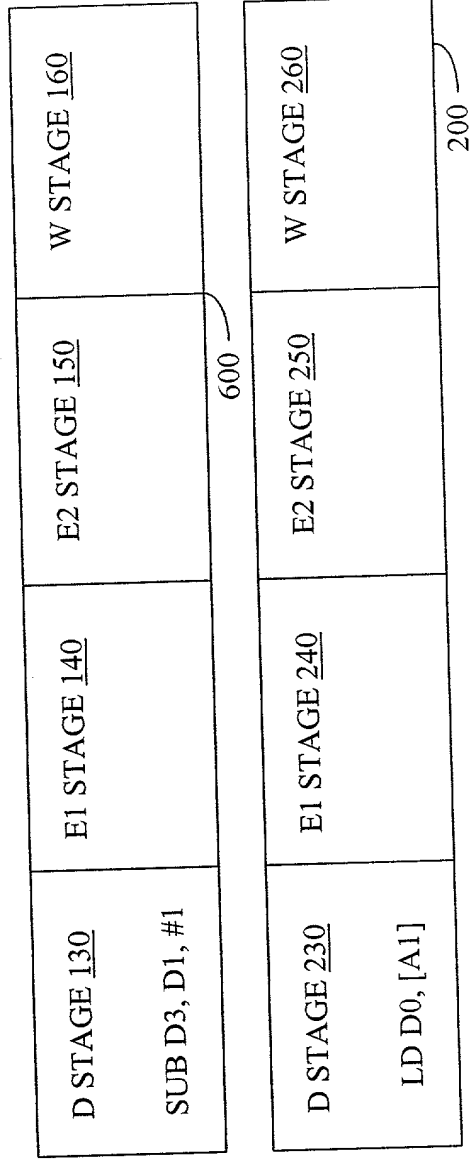


Figure 7(a)

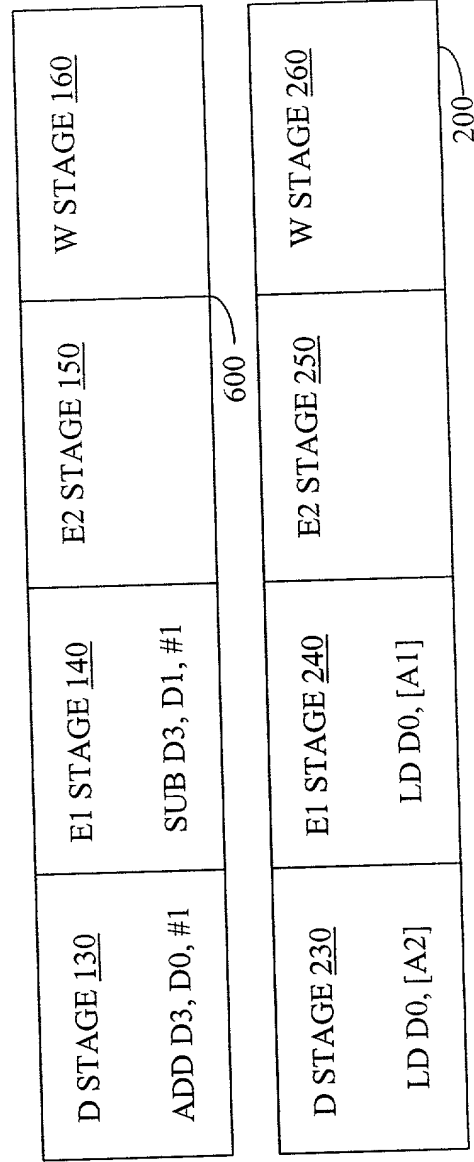


Figure 7(b)

FIG. 7(c) is a block diagram of a processor 200, according to one embodiment of the present invention. The processor 200 includes a D stage 230, an E1 stage 240, an E2 stage 250, and a W stage 260. The D stage 230 is configured to perform a data operation on a data value. The E1 stage 240 is configured to perform an execution operation on a data value. The E2 stage 250 is configured to perform an execution operation on a data value. The W stage 260 is configured to perform a writeback operation on a data value. The processor 200 also includes a D stage 230, an E1 stage 240, an E2 stage 250, and a W stage 260. The D stage 230 is configured to perform a data operation on a data value. The E1 stage 240 is configured to perform an execution operation on a data value. The E2 stage 250 is configured to perform an execution operation on a data value. The W stage 260 is configured to perform a writeback operation on a data value.

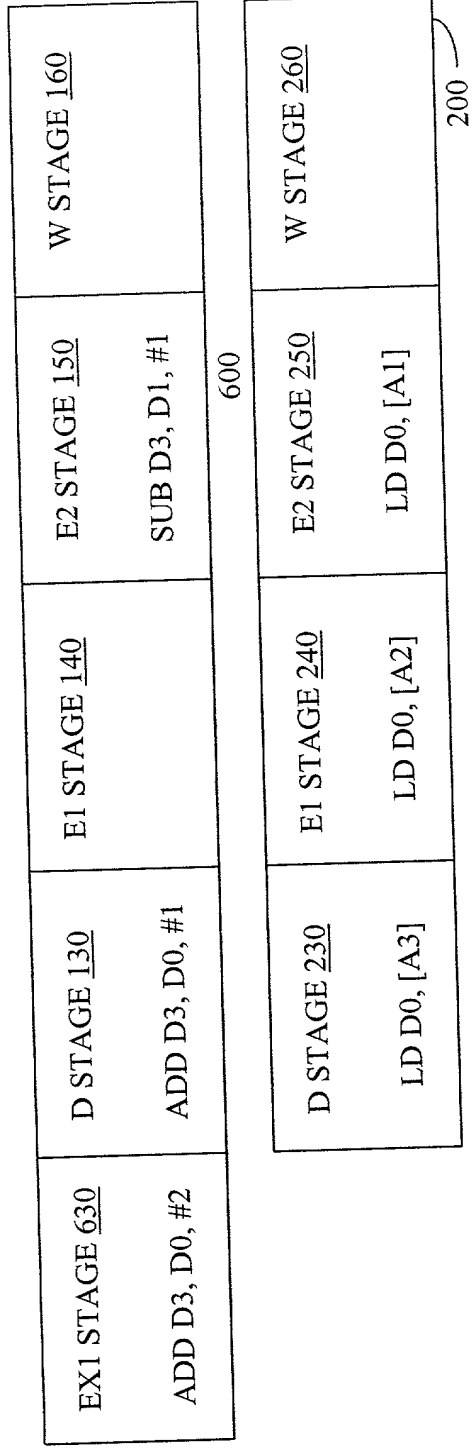


Figure 7(c)

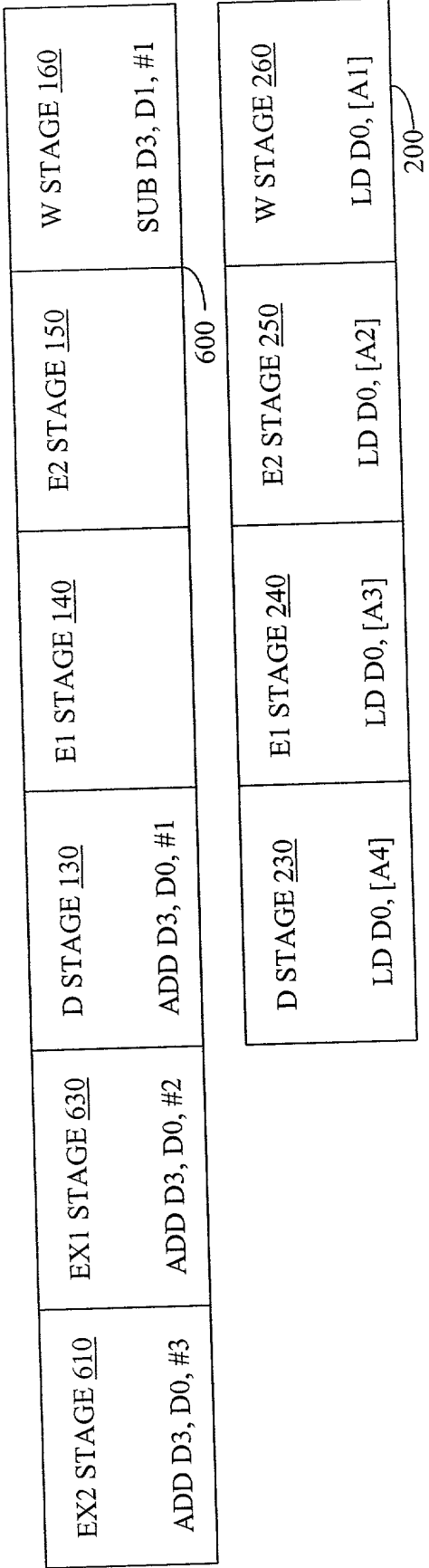


Figure 7(d)

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FIG. 7(e)

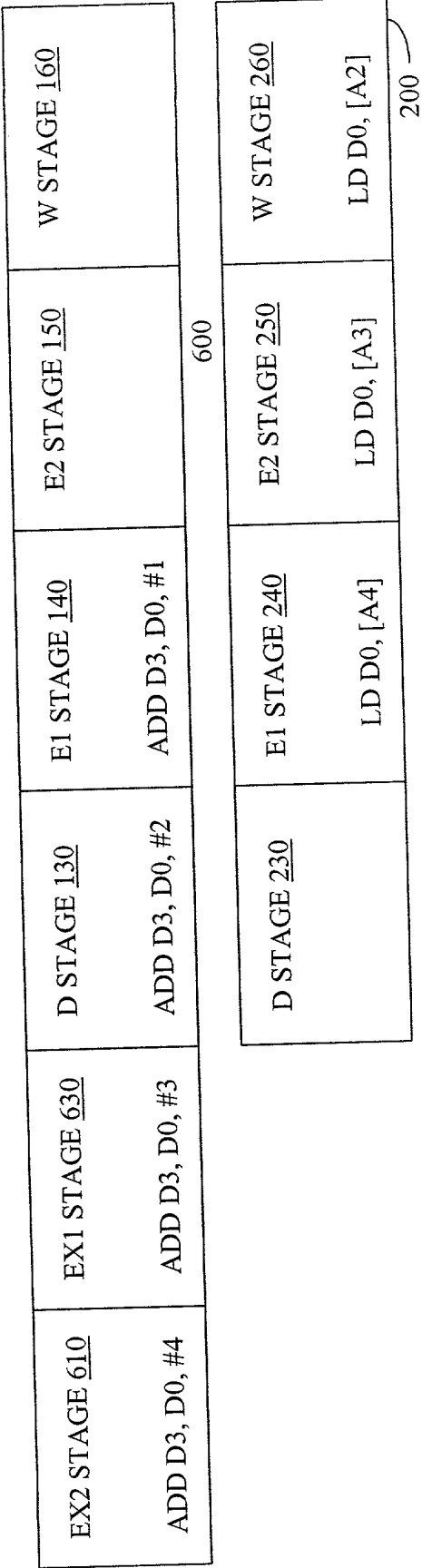


Figure 7(e)

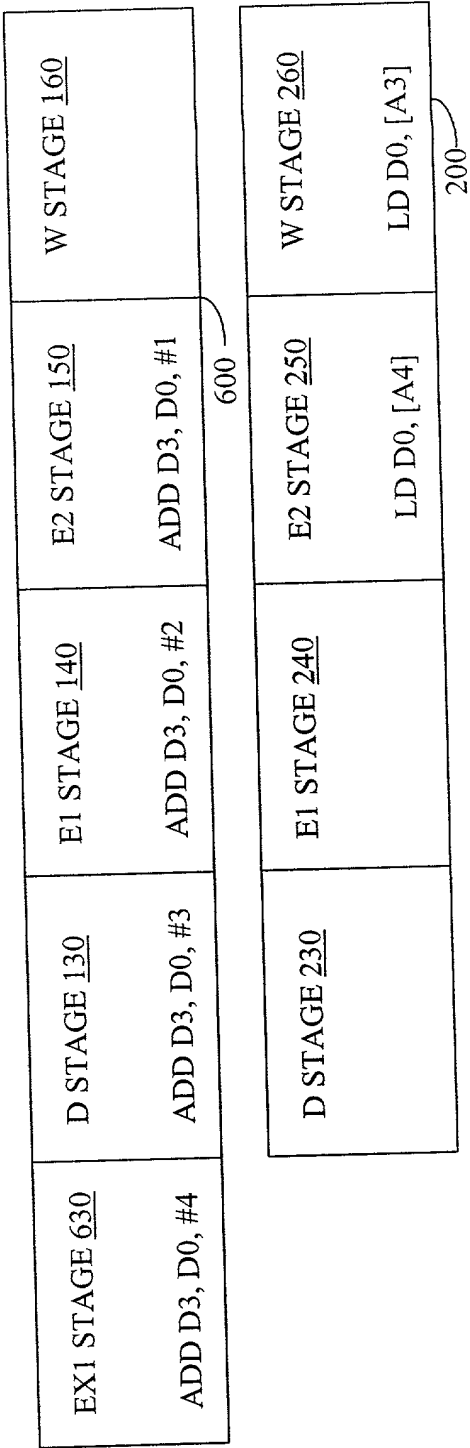


Figure 7(f)

FIG. 7(g) is a block diagram of a processing unit 200, which includes a D stage 130, an E1 stage 140, an E2 stage 150, and a W stage 160. The D stage 130 is configured to perform an ADD D3, D0, #4 operation. The E1 stage 140 is configured to perform an ADD D3, D0, #3 operation. The E2 stage 150 is configured to perform an ADD D3, D0, #2 operation. The W stage 160 is configured to perform an LD D0, [A4] operation. The processing unit 200 is connected to a bus 600.

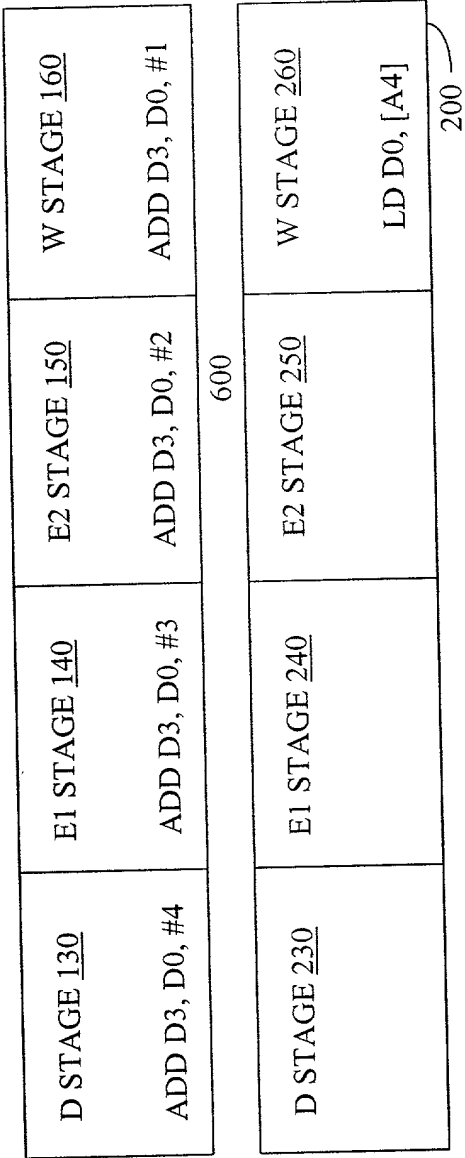


Figure 7(g)

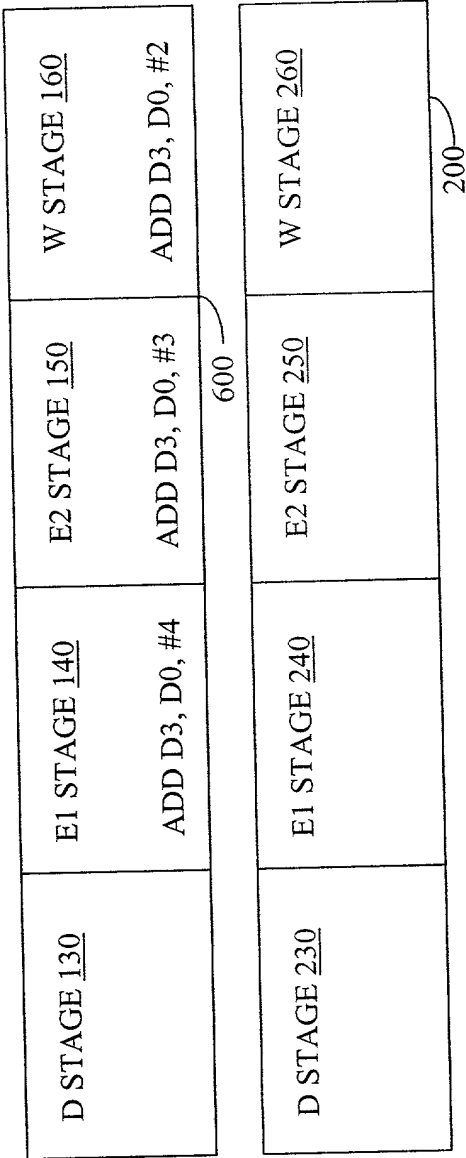


Figure 7(h)

